What is claimed is:

1. A logic dev lopment system for a built-in microcomputer that is incorporated in an electronic control unit for use, comprising:

a center block that includes an application facility and a communication facility;

a peripheral block that includes quasi microcomputer peripheral devices which simulate by software the peripheral devices of a microcomputer so as to execute an input/output process, a computing facility, and a communication facility, and that is connected to said center block over a bus;

an interface circuit block that includes circuits equivalent to the hardware of said electronic control unit, and that is connected to said peripheral block, wherein:

said communication facility included in said center block and each of said quasi microcomputer peripheral devices included in said peripheral block are connected to each other over said bus; and

said communication facility and each of said quasi microcomputer peripheral devices transfer data directly to or from each other over said bus.

2. A logic development system for a built-in microcomputer that is incorporated in an electronic control unit for use, comprising:

a center block that includes an application facility and a communication facility;

a peripheral block that includes quasi microcomputer peripheral devices which simulate by software the peripheral devices of a microcomputer so as to execute an input/output process, a computing facility, and a communication facility, and that is connected to said center block over a bus; and

an int rfac circuit block that includes circuits equivalent to th hardware of said electronic control unit, and that is connected to said peripheral

block, wherein:

said computing facility interposed between said communication facility included in said center block and each of said quasi microcomputer peripheral devices includes a bus controller;

said communication facility included in said center block and said bus controller are connected to each other over said bus, and said bus controller and each of said quasi microcomputer peripheral devices are connected to each other over an internal bus; and

said communication facility and each of said quasi microcomputer peripheral devices transfer data directly to or from each other by way of said bus, bus controller, and internal bus.

3. A microcomputer logic development system according to claim 1, wherein: a virtual input/output register is interposed between said communication facility included in said center block and said bus; and when transfer data is temporarily recorded in said virtual input/output register at the timing of receiving or transmitting data, said virtual input/output register behaves like an input/output register included in an actual microcomputer.

4. A microcomputer logic development system according to claim 1, wherein: an object on which said application facility acts is a vehicle; said logic development system includes an ignition switch; and when said logic development system is interlocked with the on or off state of said ignition switch, control software for said vehicle is initiated or terminated in the same manner as the one residing in said actual electronic control unit.

5. A microcomputer logic development system according to claim 4, wherein: said circuits that are included in said interfac circuit block and equivalent to the hardware of said electronic control unit include at least on facility circuit in which a microcomputer is

incorporat d; and said facility circuit is not actuated with the on state of said ignition switch but is actuated synchronously with the timing of starting up the center block.

6. A microcomputer logic development system according to claim 5, wherein said facility circuit includes a power circuit that is actuated with the on state of said ignition switch, and a logic circuit that when both a signal sent from said power circuit and a signal sent from said center block become valid, actuates said microcomputer.

7. A microcomputer logic development system according to claim 4, wherein: when said ignition switch is turned off, data that should be held is stored in either of a memory included in an external storage device connected to said logic development system and a memory included in said logic development system; when said ignition switch is turned on, data that should be held is read from said external storage device and restored; and the same capability as the capability of a backup memory is thus realized for said logic development system.

8. A microcomputer logic development system according to claim 4, wherein initial values to ports are set are determined within an initialization routine executed on said center block until said ignition switch is turned on after the power supply of said logic development system is turned on.

9. A microcomputer logic development system according to claim 1, wherein: said PCI bus contains a one-channel interrupt signal line over which an interrupt request is issued from said peripheral block to said center block; when said interrupt signal line is activated by said peripheral block, said application facility included in said center block accepts an interrupt request; and aft r the interrupt requ st is accept d, said int rrupt signal lin is inactivated.

10. A microcomputer logic dev lopm nt syst m

according to claim 9, wherein wh n interrupt handling is t rminated, said application facility included in said center block checks if said interrupt signal line is inactive.

11. A microcomputer logic development system according to claim 10, wherein when interrupt handling is terminated, if said interrupt signal line is active, said application facility included in said center block inactivates said interrupt signal line.

12. A microcomputer logic development system according to claim 1, wherein: said computing facility included in said peripheral block includes a facility for temporarily fetching data; when a large amount of data is transferred between said center block and each of said quasi microcomputer peripheral devices included in said peripheral block, the large amount of data is transferred in a burst mode between said center block and said computing facility, and transferred in a non-burst mode between said computing facility and each of said quasi microcomputer peripheral devices.

13. A microcomputer logic development system according to claim 9, wherein after said application facility included in said center block accepts an interrupt request, said application facility acquires interrupt flags from each of said quasi microcomputer peripheral devices over said bus; after said application facility acquires interrupt flags, said application facility clears the interrupt flags present in each of said quasi microcomputer peripheral devices.

14. A microcomputer logic development system according to claim 13, wherein after said application facility included in said center block acquires interrupt flags, said application facility executes a process associated with each of acquired interrupt flags.

15. A microcomputer logic d velopment syst m according to claim 9, wh rein: aft r said application facility includ d in said c nt r block accepts an

int rrupt requ st, said application facility acquires a plurality of interrupt flags from each of said quasi microcomputer peripheral devices over said bus; said application facility selects one interrupt flag assigned a high priority, and executes a process associated with the interrupt flag; and after the process is completed, said application facility clears a process completion interrupt flag present in each of said quasi microcomputer peripheral devices.

16. A microcomputer logic development system according to claim 15, wherein after said application facility selects one interrupt flag assigned a high priority, and executes a process associated with the interrupt flag, said application facility re-acquires a plurality of interrupt flags from each of said quasi microcomputer peripheral devices over said bus.

17. A microcomputer logic development system according to claim 13, wherein said interrupt flags are concurrently stored at successive addresses in one of registers included in each of said quasi microcomputer peripheral devices.

18. A microcomputer logic development system according to claim 17, wherein: a plurality of peripheral blocks is included; interrupt flags representing interrupts caused by each of resources that are included in each of said peripheral blocks are stored in a register included in each of said peripheral blocks; the interrupt flags representing interrupts caused by each of the resources included in the first peripheral block are stored in the register included in the first peripheral block; and an extension interrupt flag indicating whether interrupt flags, representing interrupts caused by each of resources included in each of the remaining peripheral blocks, are present is stored in association with ach peripheral block.

19. A microcomputer logic dev lopment syst m according to claim 18, wh rein if said extension

int rrupt flag demonstrates that int rrupt flags are stored in the register included in any of the remaining peripheral blocks, said application facility acquires the interrupt flags from the register in the remaining peripheral block.

20. A microcomputer logic development system according to claim 1, wherein: a plurality of peripheral blocks is included; the first peripheral block alone includes a free-run timer; said first peripheral block includes at least resources that act synchronously with the timer value of said free-run timer; and the remaining peripheral blocks include resources independent of said free-run timer.

21. A microcomputer logic development system according to claim 20, wherein: the resources that act synchronously with the timer value of said free-run timer include a comparator and a capture unit; and the resources independent of said free-run timer include a pulse-width modulator (PWM), a communication unit, an A/D converter, and ports.

22. A logic development system for a built-in microcomputer that is incorporated in an electronic control unit for use, comprising:

a center block that includes an application facility;

a peripheral block that includes quasi peripheral devices which simulate the peripheral devices of a microcomputer so as to execute an input/output process; and

a bus over which said center block and said peripheral block are connected to each other, wherein:

when an interrupt factor occurs in any of said quasi peripheral devices, said application facility reads or writes data in or from said quasi peripheral device; and

data whose proc ssing speed is requested

to be low is read or written all tog ther during communication performed before or after the action of said application facility.

23. A logic development method for a microcomputer requiring a center block that includes an application facility, a peripheral block that includes quasi microcomputer peripheral devices which simulate by software the peripheral devices of a microcomputer so as to execute an input/output process, an interface circuit block that includes circuits equivalent to the hardware of an electronic control unit, and a bus over which said center block and said peripheral block are connected to each other, said microcomputer logic development method comprising the steps of:

issuing an interrupt request from said peripheral block to said center block over a one-channel interrupt signal line contained in said bus;

accepting the interrupt request when said interrupt signal line is activated by means of said peripheral block;

inactivating said interrupt signal line after the interrupt request is accepted.

24. A microcomputer logic development method according to claim 23, further comprising the steps of:

after an interrupt request is accepted, acquiring interrupt flags from each of said quasi microcomputer peripheral devices over said bus; and

after the interrupt flags are acquired, clearing the interrupt flags from each of said quasi microcomputer peripheral devices.